Amendments to the Specification:

Replace the title with the following new title:

"Edge Seal for Integrated Circuit Chips"

Amend paragraph [0015] as follows:

Figure 1 illustrates one embodiment of the invention. In the structure shown in Figure 1, a plurality of integrated circuits (IC) 11 have ~~has~~ been formed on substrate 10, with dicing channel 18 therebetween. Each IC 11 comprises the active device regions of the chip (not shown), interconnect wiring 12, and metal pads 13. Surrounding each ~~the~~ IC is a layer 16 of energy absorbing material which is capable of absorbing mechanical stresses imparted onto the IC 11 during assembly and packaging. A final passivation layer 17 is disposed over the layer 16 to hermetically seal the chip prior to dicing. Embedded in layer 16 are a plurality of conductive leads 14 connecting the metal pads 13 with bonding pads 15. Leads 14 may be jogged or staggered, as shown, or they may be straight. The energy absorbing material 16 contacts the sides of IC 11, in addition to the top surface of IC 11.

Amend paragraph [0023] as follows:

Next, a channel 18 is defined by conventional techniques, such as by photolithography, and is etched in the kerf region surrounding each chip 11. The channel is etched through the various layers residing on substrate 10, but is not etched through substrate 10. A planarizing layer of energy-absorbing material 16 is deposited, preferably spun on and cured, so as to at least partially fill the etched channels and to provide a ~~planarized~~ layer of this material over all active chip areas 11. Material layer 16 preferably has a thickness of about 1 to about 5 μm.

Amend paragraph [0028] as follows:

In the structure of Figure 1, the hard passivation layer 17 is terminated on the substrate 10, forming a hermetic seal on the top surface of the substrate. Figure 2 differs from Figure 1 in that the hard passivation layer 17 forms an edge seal such that it encapsulates the entire substrate 10. The structure of Figure 2 may be formed by a method similar to the method for forming the structure of Figure 1, except that the channel 18 must be etched at least partially through substrate 10, thereby exposing sidewalls of the substrate.